WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit comprising:

a first storage circuit configured to store a first value used to set a dead time;

a second storage circuit configured to store a second value used to set a pulse width;

an adder circuit configured to add the first value stored in the first storage circuit and the second value stored in the second storage circuit, thereby outputting an addition result;

a timer configured to measure an elapsed time and output a count value indicative of the elapsed time;

a first comparator circuit configured to compare the count value output from the timer with the addition result output from the adder circuit; and

a waveform-generating circuit configured to generate a pulse on the basis of a comparison result of the first comparator circuit.

2. The semiconductor integrated circuit according to claim 1, wherein the waveform-generating circuit defines a leading edge of the pulse when the first comparator circuit confirms that the count value is identical to the addition result.

3. The semiconductor integrated circuit according to claim 2, further comprising:

a third storage circuit configured to store a set value used to set a counting period of the timer; and

a second comparator circuit configured to compare the set value stored in the third storage circuit with the count value output from the timer,

and wherein the waveform-generating circuit defines a trailing edge of the pulse when the second comparator circuit confirms that the count value is identical to the set value.

4. The semiconductor integrated circuit according to claim 3, further comprising a control circuit configured to control the count value of the timer, and wherein the control circuit resets the count value of the timer to restart the timer when the second comparator circuit confirms that the count value is identical to the set value.

5. A semiconductor integrated circuit comprising:

a first storage circuit configured to store a first value used to set a dead time;

a second storage circuit configured to store a second value used to set a pulse width;

an adder circuit configured to add the first value stored in the first storage circuit and the second value stored in the second storage circuit, thereby outputting an addition result;

a third storage circuit configured to store a leading edge value used to define a leading edge of a pulse;

a selection circuit configured to select one of

the addition result of the adder circuit and the leading edge value stored in the third storage circuit;

a timer configured to measure an elapsed time and output a count value indicative of the elapsed time;

a first comparator circuit configured to compare the count value output from the timer with one of the addition result and the leading edge value selected by the selection circuit; and

a waveform-generating circuit configured to generate the pulse on the basis of a comparison result of the first comparator circuit.

6. The semiconductor integrated circuit according to claim 5, wherein the waveform-generating circuit defines the leading edge of the pulse when the first comparator circuit confirms that the count value is identical to one of the addition result and the leading edge value.

7. The semiconductor integrated circuit according to claim 6, further comprising:

a fourth storage circuit configured to store a set value used to set a counting period of the timer; and

a second comparator circuit configured to compare the set value stored in the third storage circuit with the count value output from the timer,

and wherein the waveform-generating circuit defines a trailing edge of the pulse when the second comparator circuit confirms that the count value is

identical to the set value.

8. The semiconductor integrated circuit according to claim 7, further comprising a control circuit configured to control the count value of the timer, and wherein the control circuit resets the count value of the timer to restart the timer when the second comparator circuit confirms that the count value is identical to the set value.

9. A semiconductor integrated circuit comprising:

a timer configured to measure an elapsed time and output a count value indicative of the elapsed time;

a first storage circuit configured to store a first set value used to set a counting period of the timer;

a second storage circuit configured to store a second set value used to set a pulse width of a first pulse;

an operating circuit configured to compute a value indicative of the pulse width on the basis of the first set value stored in the first storage circuit and the second set value stored in the second storage circuit;

a first comparator circuit configured to compare the count value output from the timer with the value indicative of the pulse width and computed by the operating circuit; and

a first waveform-generating circuit configured to generate the first pulse on the basis of a comparison

result of the first comparator circuit.

10. The semiconductor integrated circuit according to claim 9, further comprising:

a third storage circuit configured to store a value used to set a dead time;

an adder circuit configured to add the value indicative of the pulse width and computed by the operating circuit, to the value used to set the dead time and stored in the third storage circuit, thereby outputting an addition result;

a second comparator circuit configured to compare the count value output from the timer with the addition result of the adder circuit; and

a second waveform-generating circuit configured to generate a second pulse on the basis of a comparison result of the second comparator circuit.

11. The semiconductor integrated circuit according to claim 9, wherein the first waveform-generating circuit defines a trailing edge of the first pulse when the first comparator circuit confirms that the count value output from the timer is identical to the value indicative of the pulse width.

12. The semiconductor integrated circuit according to claim 10, wherein the second waveform-generating circuit defines the leading edge of the second pulse when the second comparator circuit confirms that the count value output from the timer is identical to the

addition result.

13. The semiconductor integrated circuit according to claim 12, further comprising:

a third comparator circuit configured to compare the first set value stored in the first storage circuit with the count value output from the timer,

and wherein the second waveform-generating circuit defines a trailing edge of the second pulse when the third comparator circuit confirms that the count value is identical to the first set value.

14. The semiconductor integrated circuit according to claim 13, further comprising a control circuit configured to control the count value of the timer, and wherein the control circuit resets the count value of the timer to restart the timer when the third comparator circuit confirms that the count value is identical to the first set value.